NANOMETER-SCALE MEMORY DEVICE UTILIZING SELF-ALIGNED RECTIFYING ELEMENTS AND METHOD OF MAKING

ABSTRACT

A memory device including a substrate, and multiple self-alignednano-rectifying elements disposed over the substrate. Each nano-rectifying element has multiple first electrode lines, and multiple device structures disposed on the multiple first electrode lines forming the multiple self-aligned nano-rectifying elements. Each device structure has at least one lateral dimension less than about 75 nanometers. The memory device also includes multiple switching elements disposed over the device structures and self-aligned in at least one direction with the device structures. In addition, the memory device includes multiple second electrode lines disposed over, electrically coupled to, and self-aligned to the switching elements, whereby a memory device is formed.